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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/585,476

07/17/2006

Wolfgang Bauer

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07/25/2008

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EXAMINER

ARBES, CARL J

ART UNIT

PAPER NUMBER

3729

MAIL DATE

DELIVERY MODE

07/25/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/585,476	Applicant(s) BAUER ET AL.	
	Examiner C. J. Arbes	Art Unit 3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) 19-27 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
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| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>herein</u> . | 6) <input type="checkbox"/> Other: _____ |

Applicants' traversal of the Office's restriction has been duly noted. The traversal is held to be not sufficient to overcome the Office's Restriction. That is using the same Noble metal on the conductor base does not satisfy the general inventive concept standard with respect to these 2 different sets of claims. The Office continues to hold that the Office's Restriction is proper. In view of this holding the Restriction is now **made Final**. Applicants are required to either cancel non-elected claims or take other appropriate action.

An Office Action on the merits of claims 1-18 now follows.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. To the extent that Applicants have consistently used the term "characterized" in each of the claims 1-18 and the Examiner does not understand what Applicants intend by using this term it is held that the claims are unclear, vague and indefinite, Applicants will either carefully explain what they intend by using this term or in the alternative rewrite the claims using term which is commonly used in U.S. patent prosecution and is understandable.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-12 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mikado et al (Pat No. 6,242,079 B1); hereinafter Mikado et al.. Mikado et al teach a method of making a multi-layered printed wiring board that includes an underlayer conductor circuit (26) , an upper layer conductor circuit (44) formed on an interlaminar insulating layer (37) and a via hole (51) connecting the underlayer to the upper layer conductor circuit (44). (Cf. Abstract) The circuit board has a roughened surface (35) by treating the underlayer conductor circuit 24 with an etching solution. Good connection reliability results. Mikado et al also teach using a metal such as Titanium, Aluminum, Zinc, Iron, Indium, Thallium, Cobalt, Nickel, Tin or a noble metal such that the via hole conductor is not disturbed (Cf. Col 12). The thickness of this metal layer ranges between 0.01-5 microns. (Cf. Col 12) Mikado et al also teach forming wiring layers on both major sides of a core board as well as a through hole in the core board. (Cf. Col 17). After the surface of the interlamnar resin is roughened it can be electrolessly plated. A noble metal ion can be applied to the roughened surface (Cf. Col 18) Thereafter a thin electroless plated film is formed on the entire surface roughened surface on which the catylyst nucleus (of noble metal) has been deposited (Cf. Col 18) The thickness of this electrolessly plated metal e.g. Copper can range between 1-5 microns. A photosensitive resin is laminated on the electrolessly plated film. The photosensitive film is subjected to light exposure and developed to provide a circuit pattern. Thereafter an electrolytic film is formed on the electrolessly formed film (Cf. Col. 19) The electrolytic Copper film's thickness ranges from 10-20 microns. It would have been obvious to provide that the noble metal colloid e.g. Palladium be rough (if in

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fact Mikado et al do not explicitly teach this limitation) inasmuch this roughness feature would provide better adherence whenever additional layers were placed onto the noble metal layer. As applied to claims 2, it is held that this limitation is within the ordinary skill of a PHOSITA and hence is given little or no patentable weight., As applied to claims 4-6, Mikado et al teach using a chemical etching means to roughen the underlayer conductor layer. The use of (a) ionic etching or (b) mechanical processing is held to be within the skill of an artisan given the Mikado et al teaching and therefore merits little or no patentable weight. As applied to claim 7 it is held that the thickness of the noble layer which Applicants claim compared with that taught by Mikado et al would have been obvious to a PHOSITA. Alternatively the range of thicknesses of the noble layer (recited in claim 7) is held to be design choice inasmuch as there is no particular purpose enunciated therefore nor is there any specific problem that is solved thereby. As applied to claim 9-11 inasmuch as Mikato et al teach using an electroless method of applying the noble metal layer it is held to within the ordinary skill of a PHOSITA to use instead, an electroplating or a cathodic evaporation or a sputtering method to apply the noble metal to the conductor layer inasmuch as these last 3 methods are conventional in this art.

Claims 13 and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Mikado et al in view of Hunt et al (Pat No. 6,500,350 B1); hereinafter Hunt et al.

The teaching of Mikado et al has been described above and is not repeated. Hunt et al teach the formation of thin film resistors embedded in printed circuit boards. Resistive materials that can be used are platinum , silica and alumina (Cf. Col 5) The

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resistive material can be deposited by means of combustion chemical vapor deposition (CCVD) Exposed and developed photoresist can be used to form discrete patches of resistive material. The resistive material can be deposited onto metal e.g. copper foil. (Cf. Col 6) It would have been obvious to combine the teaching and to provide resistors onto the wiring board taught by Mikado et al inasmuch as this would give utility to the board. Moreover it would be within the ordinary skill of this art for a PHOSITA to try to create a wiring board having printed resistors on the wiring board layers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to C. J. Arbes whose telephone number is 571-272-4563. The examiner can normally be reached on M, T, R and F from 8 to 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, P. Vo, can be reached on (571) 272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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/C. J. Arbes/
Primary Examiner, Art Unit 3729